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SUGHRUE MION ZINN MACPEAK & SEAS
2100 PENNSYLVANIA AVENUE NW
SUITE 800
WASHINGTON, DC 200373213

EXAMINER
PHILPOTT, JUSTIN M

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 02/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/242,822	FICHE, GEORGES	
	Examiner	Art Unit	
	Justin M Philpott	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/18/2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 December 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office action is in response to the Amendment filed December 18, 2002.

Response to Amendment

1. Regarding the specification, Applicant has amended the specification in response to the requirement for FIG. 4B to be designated by a legend such as --Prior Art-- with which Applicant disagrees. However, new matter has been added. Particularly, at page 6 Applicant has added "Figure 4B showing a device according to the invention and *which allows wide band transfers*, this latter device being able to be derived from incomplete prior art matrices and by restricting routing in these derived prior art matrices *to allow broadband transfers* (Figure 4B) *and narrowband transfers* (Figure 4A)". The specification as originally filed did not disclose a device which specified allowing wide band transfers. Thus, such a statement is considered new matter and the specification remains objected to. Furthermore, when Figure 4B is configured to "allow narrowband transfers (Figure 4A)", according to the specification as amended it is in fact configured according to Figure 4A which is clearly prior art. Thus, such a configuration of Figure 4B to allow narrowband transfers as described is prior art. Applicant may maintain Figure 4B is part of the present invention by removing the above-italicized "which allows wide band transfers" and "and narrowband transfers (Figure 4A)". Otherwise, Applicant is required to designate Figure 4B as prior art. The typographical corrections made to the specification (page 7 and 8) are approved.

2. Applicant has requested the Examiner to recheck Applicant's file for a copy of the certified copy of the priority document. Such a document has been identified and is present in Applicant's file.

Response to Arguments

3. In the Office action of September 18, 2002, the drawings were objected to because Figures 1, 4A and 4B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Claims 1 and 4 were rejected under 35 U.S.C. 102(b) as being anticipated by Wong, and claims 2, 3 and 5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view Petersen. In the Amendment, Applicant designates Figures 1 and 4A as prior art, and amends claims 1 and 3 to correct typographical errors. Also, Applicant argues that Figure 4B is part of the present invention and should not be labeled as prior art, and further traverses the rejections of claims 1-5.

4. Applicant argues that Fig. 4B is not prior art, and thus, should not be labeled as such. Applicant's argument has been considered and Fig. 4B will not be required to be designated by a legend such as --Prior Art-- if Applicant makes appropriate changes to the specification as discussed above in "Response to Amendment".

5. Applicant's arguments, filed December 18, 2002, regarding the rejection of claims 1 and 4 under 35 U.S.C. 102(b) as being anticipated by Wong have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that the reference used to show Wong teaches setting the value of m equal to n for the m x n matrix is directed to the three-stage architecture of Fig. 2, and thus, is not directed to the two-stage architecture of Fig. 1. The reference to Fig. 2, however, was made to indicate a configuration known in the art which specifically utilizes values of m equal to n. Further explanation of Wong teaching setting the value of m equal to n, however, is provided in the following. Applicant further argues that Wong teaches away from having m=n by stating that it is preferred to have the ratio e=m/n to be greater than 1. Wong, however, does *not* teach away from having m=n. Rather, with respect to Figure 1, Wong discloses three different techniques are used in the art to reduce the loading within the switching fabric, only one of which comprises having values of m greater than n. A first technique involves providing buffers at the output of a first-stage switch (page 708, col. 2, lines 4-5). A second technique is called "grouping" (lines 3-8) wherein more than one line, e.g. *r* lines, is provided for each path between the two stages. Wong discloses that the grouping technique is often preferred for reducing the possibility of congestion (lines 7-8). Wong further discloses a third technique called "input-expansion" (lines 9-16) wherein the ratio e=m/n is designed to be greater than 1. Wong notes that r and e are in fact related wherein if the value of r is adjusted, the value of e should also be adjusted in order to maintain comparable performance. While Wong uses an example of having a group size r=8 and choosing a corresponding input-expansion e=2 to provide close to 100% throughput for the given group size, r and e values are not limited to this first example. The teachings of Wong in fact are directed towards reducing the input-expansion ratio, e, while achieving comparable packet loss performance (page 710, col. 1, lines 1-5), which reduces the amount of hardware interconnections. In the invention of Wong (Figure

4), the two-stage architecture of Figure 1 configured with first-stage and second-stage switching grouped into partitions (e.g., Figure 3; see also page 709, col. 2, lines 4-6), yielding a three-stage Dilated-Banyan switch, is utilized with the addition of an overflow switch (v x v, see Figure 4). Wong specifies m is set to be greater than *or equal* to n (page 710, col. 1, lines 8-10) and further discloses a simulation wherein e=1 (i.e., m=n) in Table 1(a) (page 711). Thus, Wong clearly teaches an embodiment as described in claim 1 wherein the value of m is equal o the value of n.

Applicant further argues that Wong does not disclose the requirement in claim 1 that "each input ... of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs ... exclusively associated with that input; and that each output ... of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs ... of the outlet stage exclusively associated with that output". Wong, however, does in fact disclose the above requirement of claim 1. Wong teaches *grouping* (see Figure 1) wherein more than one line, e.g. *r* lines, selected from a particular grouping of r lines, are provided for each path between the inlet and outlet stages. That is, Wong teaches each input of the inlet stage (n) can be connected to an output of the inlet stage (at m, one of the lines of a corresponding grouping of r lines) selected from only Q outputs (r outputs) exclusively associated with that input (n); and that each output of the outlet stage (p) can be connected to an input of the outlet stage (at s, one of the lines of a corresponding grouping of r lines) which can be selected only from Q' inputs (r inputs) of the outlet stage exclusively associated with that output (p).

Regarding claim 4, Applicant argues that the rejection is based upon an assumption that n'=1, and Wong lacks sufficient specificity to constitute such an anticipation. While the

teachings of Wong do not require specifically n=1 or n'=1, Figure 3 accommodates such an embodiment as evidenced by " ..." between the first (1) and kth (k) inputs, outputs, etc. That is, Figure 3 is not limited to a specific number of inputs, outputs, etc. Moreover, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Furthermore, in reference to the language of claim 4, "each of the inlet stage has single input and R outputs", using the above-mentioned grouping method, Wong provides each single input (n) having R outputs (r or r').

6. Applicant's arguments, filed December 18, 2002, regarding the rejection of claims 2, 3 and 5 under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Petersen have been fully considered but they are not persuasive.

Applicant argues that the current grounds of rejection do not present the required showing that the claimed invention would have been obvious in view of the combination of Wong and Petersen. Wong teaches various architecture for ATM switching, and particularly for fast-packet switching in order to provide widespread use of broadband communications. Wong identifies the primary goals for ATM switching which include: minimizing the number and size

of the switches needed, maintaining high throughput and low loss probability, and maintaining packet sequence (page 708, col. 1, "Introduction"). Wong attempts to achieve as much of these goals as possible using three-stage banyan architecture with overflow switching. Petersen also recognizes the need for improved ATM switching (col. 1, line 9 – col. 2, line 39) and states that while other prior art is oriented towards developing switchcores of greater magnitude (including banyan related architecture coupled with buffering, as taught by Wong) in order to meet demands of, for example, broadband communication, a need exists for access control to improve size, capacity/throughput, and loss problems (col. 2, lines 24-39) commonly experienced with this existing art. In particular, the invention of Petersen eliminates the need for large buffers in the switchcore (col. 3, lines 13-17), reducing size requirements. Additionally, Petersen teaches a switchcore matrix having a plurality of rows, columns and crosspoints for providing both multicast and broadcast capabilities (col. 2, lines 42-62), significantly improving capacity/throughput. Further, Petersen teaches a switchcore matrix with access control and wherein a plurality of switchcore matrixes are link-coupled to enhance switch performance (col. 2, lines 58-62), wherein cell loss probability can be reduced and control can be provided for maintaining packet sequence. Finally, the invention of Petersen provides simplicity such that it may be constructed on a single integrated circuit, making it ideal for manufacture and application. Thus, the access control and crosspoint features of the invention of Petersen clearly provide improvements over Wong, wherein the goals specified by Wong are achieved by Petersen resulting in significant improvements in ATM switching. Accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings

of Petersen to the device of Wong in order to provide improved ATM switching as discussed above.

Claim Rejections - 35 USC § 102

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's cited document by Wong et al.

Regarding claim 1, Wong teaches devices for switching ATM cells (figures 1, 3 and 4; primary reference is made to the general architecture of figure 1 by which figures 3 and 4 are based upon) establishing a single path per virtual circuit having N.R inputs (k.n inputs) and N.R outputs (l.p outputs), N and R (k or l, and n or p) being two integers not less than two, the device comprising at least two stages, including an inlet stage (n x m stage) having R.N sets (n.k sets) of Q outputs (r) and an outlet stage (s x p stage) having R.N sets (p.l sets) of Q' inputs (r) – wherein n=p, m=n, and m=s (see page 709, col. 1, lines 4 and 17) and along the same logic k=l, thus n=m=s=p=R and k=l=N.

Furthermore, the above is characterized in that for the flow of data carried by any intermediate link (one of the links in a grouping of r links) that is part of the single path set up between an input and an output (r) to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input (n) of the inlet stage (n x m stage) can be connected to an output of the inlet stage (at m, one of the lines of a corresponding grouping of r lines) which can be selected only from Q outputs (r lines) exclusively associated with that input;

and in that each output (p) of the outlet stage (s x p stage) can be connected to an input of the outlet stage (at s, one of the lines of a corresponding grouping of r lines) which can be selected only from Q' inputs (r lines) of the output stage exclusively associated with that output (p).

Regarding claim 4, Wong teaches a switching device (figure 3) according to claim 1 including an inlet stage (n x m stage), a central stage (l x l' stage), and an outlet stage (m' x n' stage) characterized in that Q and Q' (r and r') are equal to R (see page 709, col. 2, line 17 and page 710, col. 1, line 10 wherein l=l' and m=m' and therefore r=r'=(Q=Q')=m=R), the central stage (l x l' stage) includes R^2 matrices (r=r', therefore the l x l' stage includes r^2 or R^2 matrices), and the matrices of the inlet stage and the matrices of the central stage are organized into R sets (n sets) each including N matrices (h matrices) of the inlet stage and R matrices (g matrices, where g may be equal to m) of the central stage and the matrices of the outlet stage are organized into N sets (h' sets) of R matrices (m' matrices, where m' may equal r'). Furthermore, the above is characterized in that each of the R.N matrices of the inlet stage (n x m stage) has a single input (i.e., the first/top input at n) and R outputs (r lines), each of the R^2 matrices of the central stage has N inputs and N outputs (l inputs and l' outputs) – the inputs being respectively connected to an output of each of the matrices of the inlet stage that belong to the same set of matrices, and each of the R.N matrices of the outlet stage (m' x n' stage) has R inputs (r' lines) and a single output (i.e., the first/top output at n'), those R inputs (r' inputs) being connected to outputs respectively belonging to the R sets of matrices of the central stage and of the inlet stage.

Claim Rejections - 35 USC § 103

9. Claims 2, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of U.S. Patent No. 5,467,347 to Petersen.

Regarding claim 2, Wong teaches the device described (see the above regarding figure 1) with the exception that Wong does not specifically disclose each matrix having exactly R.N outputs (n.k outputs) organized into R sets (n sets) of N outputs (k outputs) with each set corresponding to a respective one of the R inputs (n inputs). Rather, the device taught by Wong comprises matrices having m outputs wherein m is greater than or equal to n and wherein m does not necessarily correspond to exactly n sets of k outputs.

Petersen teaches improvements for ATM switching means wherein an inlet stage (switchport 11, see FIG. 1) is coupled to a plurality of outlet stages (switchcore 12 having planes a and b) wherein each matrix of the inlet stage (switchport 11) has outputs organized into a number of sets (one in this example) of N (n) outputs (n=2 in this example). Applying this configuration of Petersen to an ATM switching device allows for implementation on a single chip and greatly reduces hardware and maintenance costs while increasing reliability (see col. 5, lines 20-35). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the ATM switching arrangement of Petersen to the ATM switching device of Wong in order to reduce cost and increase reliability.

Regarding claim 3, Wong teaches a switching device (figure 2) according to claim 1 including an inlet sage (n x m stage), a central stage (k x k stage), and an outlet stage (m x n

stage) characterized in that, Q being equal to R (n), the inlet stage comprises N (k) matrices each having R (n) inputs each of which can be connected to an output of that matrix which can be selected only from R (m, or n wherein m=n; see page 709, col. 1, line 17) outputs of the set of outputs corresponding to that input, and the central stage (k x k) comprises a set of R (m) matrices each having N (k) inputs and N (k) outputs wherein the R (m) outputs of each set of outputs of the inlet stage are connected to inputs belonging to the same set of R (k) matrices of the central stage.

Furthermore, the above is characterized in that, Q' being equal to R (n), the outlet stage comprises N (k) matrices each of which have R (m) inputs and R (n) outputs, wherein each output of a matrix can be connected to an input of that matrix which can be selected only from R (m) inputs corresponding to that output.

However, as with claim 2 above, Wong does not specifically disclose each matrix having inputs/outputs organized into R sets of R inputs/outputs. Rather, the device taught by Wong comprises matrices having m outputs with a single set of inputs/outputs in each matrix of each stage. Therefore, Wong does not specifically teach each matrix of the inlet stage having R^2 outputs, or R sets of R outputs, and likewise does not teach R sets of R matrices in the central stage or R^2 inputs in each matrix of the outlet stage.

As discussed above, Petersen teaches improvements for ATM switching means wherein the inlet stage (switchport 11) has R^2 outputs, or b sets of n outputs (wherein b=2 and n=2, in FIG. 1). Such an arrangement reduces cost and increases reliability and can be advantageously applied to the device taught by Wong to provide these improvements. Having R^2 outputs in the inlet stage, the device of Wong in view of the teachings of Petersen would further comprise R

sets of R matrices in the central stage and similarly R^2 inputs in each matrix of the outlet stage in order to provide the desired ATM switching taught by Wong with the improvements in ATM switching taught by Petersen. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the ATM switching teachings of Petersen to the ATM switching device of Wong in order to provide a more robust ATM switching device with reduced cost and increased reliability.

Regarding claim 5, the device of Wong in view of Petersen teaches a switching device according to claim 3 as discussed above. Furthermore, such a device having three stages may advantageously be implemented with N and R values such that $N=2.R^2$.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703.872.9314 for regular communications and 703.872.9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.4750.

Justin M Philpott

January 28, 2003

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600